Abstract of Disclose

A delay locked loop device includes a first delay line for receiving an external clock signal and a first delay control signal to generate a first internal clock signal; a second delay line for receiving the external clock signal and a second delay control signal or the first delay control signal to generate a second internal clock signal; a first delay control block for receiving the external clock signal to generate the first delay control signal; a second delay control block for receiving the external clock signal to generate the second delay control signal; and a phase detecting block for receiving the first internal clock signal and the second internal clock signal to generate the on-off signal by comparing a phase of the first internal clock signal with a phase of the second internal clock signal.